Electron Beam Crystallization of Amorphous Silicon Thin Films

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Abstract

A promising method for low cost production of efficient silicon thin film solar cells is the electron beam physical vapor deposition (EB-PVD) of high purity amorphous silicon (a-Si) layers with high deposition rates up to 300 nm/s [1] followed by crystallization [2]. Both steps could be part of a sophisticated approach for an innovative kerfless wafering cycle process [3] (Figure 1-a). Due to the ability to adjust the power-depth relation (Figure 1-b), an epitaxial regrowth could be reached by using EB technology at the crystallization step. This study focuses on EB crystallization of deposited a-Si films in the solid phase regime and justifies observed experimental results by simulations. For experiments, a focused EB was moved over a-Si coated substrates. Processing a 1 µm thick a-Si layer with planar scanning pattern led to slow heating up to 1500 K of the whole sample. After this procedure, the layer is still attached and an epitaxial regrowth with substrate crystal orientation occurred. In contrast, additional short time crystallization tests were carried out by moving the EB along a line. Lower scanning speeds, corresponding to large energy input, leads to a fine-grained crystallization and to an undesired delamination of the layer, whereby with increasing scanning speeds delamination occurs only at certain areas and disappears completely if the scan speed exceeds 50 m/s. Simulations were carried out to clarify delamination phenomena. Therefore, a 3D model with a swept mesh was generated, representing the substrate-layer-system (Figure 2). In a coupled study using the Heat Transfer and Structural Mechanics Modules of COMSOL Multiphysics® software the transient temperature field and thermal induced stress were calculated. The applied EB line pattern was considered as a moving heat source with a spatial distribution according to the absorbed EB power-depth-relation in Figure 1-b. Initial layer tensile stress of 200 MPa, a common value [4], was also taken into account.
Figure 3 shows that the maximum temperature is below the melting point of a-Si (1420 K [5]).Therefore, the initiation of crystallization would not be expected in contrast to experimental results. But considering the elastic strain energy (Figure 4) for lower speeds < 50 m/s, calculated values exceed the a-Si/c-Si interface energy [6]. That means during the experimental EB line processing the a-Si layers spall off due to high elastic energy. Layer crystallization took place after spalling off because of lower thermal coupling to the c-Si substrate and hence stronger layer heating. The shown introductory investigations are a part of a research project for kerfless wafering funded by the European Union and the Free State of Saxony (funding reference 100102018). Associating crystallization tests demonstrate that an epitaxial regrowth can be reached by EB processing. Enhancing throughput's ability by increasing the a-Si thickness and intensifying EB power density

leads to undesired layer delamination. To determine process limits, e.g. layer thickness or EB exposure time, further studies have to be carried out systematically. With additional investigations, the encouraging results could be used for an industrial implementation of an innovative fabrication of Si thin films.

Reference

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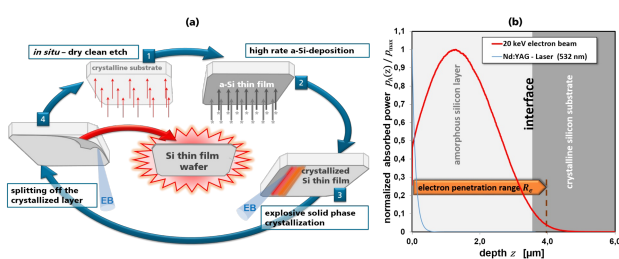
Figures used in the abstract

Figure 1: (a) Concept for kerfless wafering using electron beam (EB) technology in a cycle process, consisting of cleaning a crystalline substrate, depositing an a-Si layer on it, crystallizing the a-Si layer and finally splitting off the crystallized layer [7]. The crystalline substrate, e.g. silicon or sapphire wafer, will be reused. (b) For crystallization, the depth relation of the absorbed power in a thin-film system can be easily tuned for EB (red) by acceleration voltage in contrast to laser (blue).
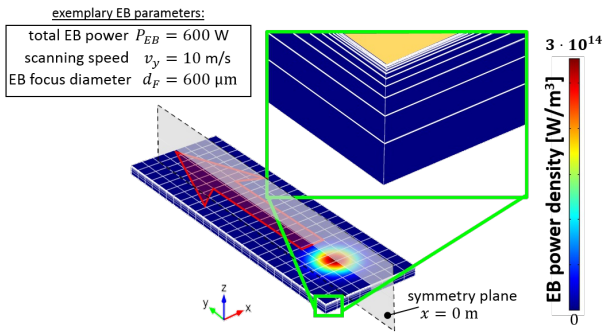
Figure 2: Used geometry with swept mesh and moving heat source due to EB treatment. For the c-Si-substrate (blue) and the 3.6 μm thick a-Si layer (yellow) different material parameters and initial stresses were implemented.
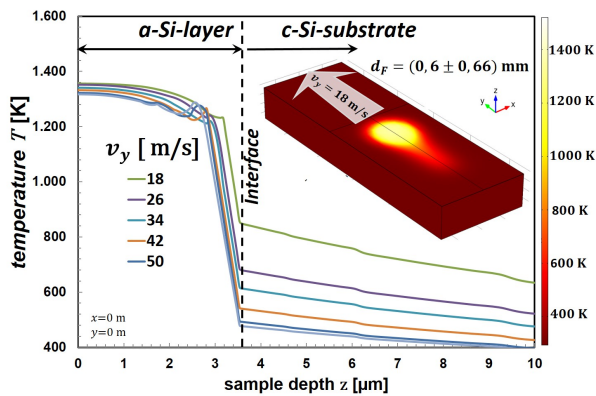

Figure 3: Calculated temperature-depth profile in a-Si/c-Si layer system during EB spot passing for various line scanning speeds. Inset: computed temperature field at a line scanning speed of 18 m/s.
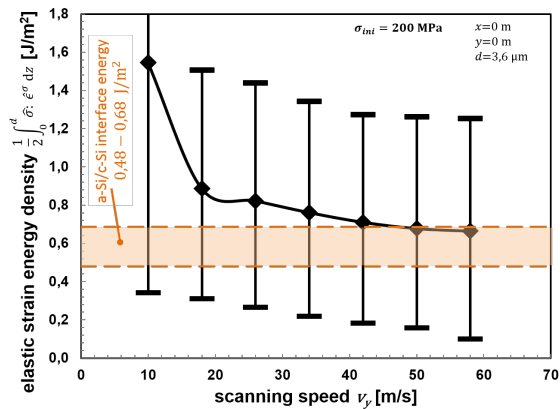

Figure 4: Calculated elastic strain energy density vs. applied scanning speed. The value range of the a-Si/c-Si interface energy [6] are highlighted for reference.